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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of: **FUKASAWA, et al.**

Group Art Unit: **2827**

Serial No.: **09/635,124**

Examiner: **GRAYBILL, David E.**

Filed: **August 8, 2000**

P.T.O. Confirmation No.: 4720

For: **METHOD AND MOLD FOR MANUFACTURING SEMICONDUCTOR DEVICE, SEMICONDUCTOR DEVICE, AND METHOD FOR MOUNTING THE DEVICE**

AMENDMENT UNDER 37 CFR §1.111

Commissioner for Patents
Washington, D.C. 20231

November 27, 2002

Sir:

In response to the Office Action dated **August 28, 2002**, please amend the above-identified application as follows:

IN THE CLAIMS:

Please cancel claims 37-39 and 45-53 without prejudice or disclaimer.

Please amend claims 12, 27-29, 32-34, 40, 65, 68, 88 and 90 as follows:

12. (Twice Amended) The method for fabricating the semiconductor device as claimed in claim 1, wherein:

the film used in the resin sealing step is formed of an elastically deformable substance, and the ends of the protruding electrodes are caused to fall in the film when the resin layer is formed by

using the mold; and

the film is detached from the resin layer in the protruding electrode exposing step so that the ends of the protruding electrodes can be exposed from the resin layer.

27. (Twice Amended) The method for fabricating the semiconductor device as claimed in claim 1, wherein:

cutting position grooves are formed, before the resin sealing step is carried out, in the substrate so as to be located in positions in which the substrate is cut in the separating step; and

the substrate is cut in the cutting position grooves after being filled with the sealing resin.

28. (Twice Amended) The method for fabricating the semiconductor device as claimed in claim 1, wherein:

a pair of stress relaxing grooves is formed, prior to the resin sealing step, so as to sandwich a position in which the substrate is to be cut; and

the substrate is cut in a position interposed between the pair of stress relaxing grooves in the separating step.

29. (Amended) A method for fabricating semiconductor devices comprising:

a first separating step of cutting a substrate on which semiconductor elements having protruding electrodes are formed so that the semiconductor elements are separated from each other;

a resin sealing step of arranging the separated semiconductor elements on a base member and sealing a sealing resin so that a resin layer is formed;

a protruding electrode exposing step of exposing at least ends of the protruding electrodes from the resin layer; and

a second separating step, conducted after said protruding electrode exposing step, of cutting the resin layer together with the base member in positions between adjacent semiconductor elements, so that the semiconductor elements to which the resin layer is formed are separated from each other.

32. (Twice Amended) The method for fabricating the semiconductor device as claimed in claim 1, wherein positioning grooves are formed on a back surface of the resin layer of the substrate after the resin sealing step is executed and before the separating step is executed.

33. (Twice Amended) The method for fabricating the semiconductor device as claimed in claim 32, wherein the positioning grooves are formed by subjecting the back surface to half scribing.

34. (Twice Amended) The method for fabricating the semiconductor device as claimed in claim 1, wherein:

the film used in the resin sealing step has projection or recess portions located in positions in which the film is not interfered with the projecting electrodes; and

recess or projection portions formed on the resin layer by the projection or recess portions

are used for positioning after the resin sealing step is completed.

40. (Twice Amended) The method for mounting the semiconductor device as claimed in claim 37 wherein the semiconductor device has an interposer having an outer connection means, and wherein an interval between the outer connection means is wider than an interval between the protruding electrodes.

65. (Amended) A method for fabricating a semiconductor device comprising:

an electrode plate forming step of forming a pattern on a metallic base so that an electrode plate is formed;

a chip mounting step of mounting semiconductor elements on the electrode plate and electrically connecting the semiconductor elements thereto;

a sealing resin forming step of forming a sealing resin which seals the semiconductor elements and the electrode plate; and

a cutting step of cutting the sealing resin and the electrode plate at boundaries between adjacent ones of the semiconductor elements so that the semiconductor devices are separated from each other,

wherein said sealing resin forming step is conducted by providing a film between said electrode plate and a mold.

68. (Twice Amended) The method for fabricating the semiconductor device as claimed in claim 65, wherein:

a chip attachment step of positioning the semiconductor elements on a heat radiating member and attaching the semiconductor elements thereto before the chip mounting step is executed; and

the semiconductor elements attached to the heat radiating member are mounted to the electrode plate in the chip mounting step,

88. (Amended) A method for fabricating the semiconductor as claimed in claim 4, wherein the resin sealing step further comprises a film disposing step of providing a non-adhesive process film between contact surfaces of the upper mold and the first lower mold half body and the second lower mold half body.

90. (Amended) A method for fabricating a semiconductor device comprising:

a mold preparing step of preparing a mold including a first mold, and a second mold which is located so as to face the first mold, the second mold including a first half body having a shape corresponding to a shape of a substrate, and a second half body which is provided so as to surround the first half body and can be elevated with respect to the first half body, the first and second half bodies cooperating with each other so that a cavity to be filled with resin is defined;

a resin sealing step of placing the substrate on which a plurality of semiconductor elements equipped with protruding electrodes are formed in the mold and supplying resin to positions in which the protruding electrodes are provided so as to form a resin layer which seals the protruding

electrodes and the substrate;

a protruding electrode exposing step of exposing at least end portions of the protruding electrodes from the resin layer; and

a separating step of cutting the substrate together with the resin layer so that the semiconductor elements are separated into each other,

wherein the resin sealing step disposes a film between the protruding electrodes and the mold, which thus contacts the sealing resin through the film.

REMARKS

Claims 1, 4, 5, 7-10, 12, 21, 22, 24-29, 32-35, 40, 65-69, 78, 86 and 88-90 are pending. Claims 37-39 and 45-53 are canceled without prejudice or disclaimer and claims 12, 27-29, 32-34, 40, 65, 68, 88 and 90 are amended. A marked-up version showing the changes made by the present amendment is attached hereto as "**Version with markings to show changes made**."

Claims 12, 27, 28, 32/30, 40, 45-53 and 33/32/30 were rejected under 35 U.S.C. §112, second paragraph, as being indefinite. Favorable reconsideration is requested in view of the amendments made herein.

Claims 12, 32/30, 40, 45-53 and 33/32/30 were considered incomplete since they depend from canceled claims. Claim 12 has been amended to depend from claim 1.

Claim 32 had depended from claim 1 or claim 30. As such, claim 32 has been amended to depend only from claim 1.

Claim 40 had depended from claim 18 or claim 36. However, in the Examiner's amendment dated November 6, 2001, its dependency was changed to claim 37. As such, it appears that the Examiner overlooked the Examiner's amendment. Claim 40 is amended to reflect the Examiner's Amendment.

Claims 45-53 directly or indirectly depend from claim 44 which had been canceled. Claims 45-53 are canceled.

The Examiner has also noted a lack of sufficient antecedent basis in claims 27, 28, 68 and 88. The claims have been amended to overcome the rejection.

The Examiner also considers claim 33 indefinite since it relates to a potential process limitation. This portion of the rejection has been overcome by changing "can be" to read -- are --.

Claims 1 and 35 were rejected under 35 U.S.C. §102(e) as being anticipated by Lim. This rejection is respectively traversed.

Lim fails to teach the feature of "the mold, which thus contacts the sealing resin through the film." In Lim, "a mold" directly contacts with the "sealing resin." Accordingly, claims 1 and 35 are not anticipated by Lim.

Furthermore, since the mold urges the sealing resin via the film in the present invention, there is no problem such as the sealing resin adhering to the mold, and the sealed substrate is easily taken out from the mold, even in the case of using a large-diameter wafer as the substrate.

Claims 4 and 88 were rejected under 35 U.S.C. §103(a) as being unpatentable over Lim further in combination with Ohta. Ohta fails to provide the teachings which Lim lacks, i.e., the feature of claim 1 of "the mold, which thus contacts the sealing resin through the film."

Claim 5 was rejected under 35 U.S.C. §103(a) as being unpatentable over Lim further in combination with Ohta, and claims 7 and 8 were rejected under 35 U.S.C. §103(a) as being unpatentable over Lim and further in combination of Ota (JP 5343458). Since these claims depend from claim 1, and Ohta as well as Ota each fail to teach the features which Lim lacks as noted above, claims 5, 7 and 8 also are patentable.

Claims 1, 24, 25 and 34 were rejected under 35 U.S.C. §103(a) as being unpatentable over the combination of Kihira and Tanaka. Favorable reconsideration of this rejection is earnestly solicited.

The Examiner acknowledges that Kihira does not teach a resin sealing step which disposes a film between the protruding electrodes and the mold which thus contacts the sealing resin through the film. Tanaka is applied by the Examiner for allegedly providing this teaching. In particular, Tanaka provides a protective member 17 which is separably adhered to a predetermined face of each electrode 12 to be exposed after sealing. It is respectfully submitted that the combination of these references fails to teach or suggest the claimed invention.

Tanaka discloses the process of sealing a chip by a resin together with a protective member 17. Tanaka further teaches moving the protective member 17 thereafter. On the other hand, Tanaka is entirely silent about the "film" as taught in claim 1 of the present invention.

In Tanaka, it is necessary to align the contact part of the chip with the projecting part of the protective member, while no such alignment process is necessary in the present invention that uses a film.

It is further noted that the Tanaka uses transfer molding. Thus, in the event a film is used in place of the protective member 17 in Tanaka, the resin would not reach the side of the wafer surface on which the contact is formed because of the too narrow gap formed between the chip surface carrying the contact and the film. Thus, it is impossible in Tanaka to achieve resin sealing by using a film as proposed in the present invention.

Thus, it is essential in Tanaka to use a protective member having a projection for securing

sufficient space for resin flow, while this teaching is contradictory with the use of a film as set for in amended claim 1. Associated with the use of the projection, the alignment process noted before is also essential in Tanaka.

Claim 29 was rejected under 35 U.S.C. §102(b) as being anticipated by Badehi. Favorable reconsideration of this rejection is requested in view of the amendments made herein.

More specifically, claim 29 has been amended to clarify that the second separating step is conducted after the protruding electrode exposing step. In contrast thereto, Badehi exposes the terminals at the sidewall surface. As such, the "protruding electrode exposing step" and the "second separating step" in Badehi are inevitably conducted simultaneously. On the other hand, the exposure of the protruding electrode is conducted in the state the plural semiconductor elements are sealed in the present invention.

Claims 32 and 33 were rejected under 35 U.S.C. §103(a) as being unpatentable over Lim in combination with Romano. Romano fails to provide the teachings which Lim lacks, as discussed above.

The rejection of claims 37-39 under 35 U.S.C. §102(b) as being anticipated by Yasunaga has been rendered moot by cancellation of these claims.

Claim 89 was rejected under 35 U.S.C. §102(a) as being anticipated by Kihira. This rejection is respectfully traversed.

The Examiner characterizes the molding resin 19 of Kihira as a "rigid sealing material". However, Kihira does not provide a rigid sealing material. In the wafer-level transfer molding process described in Kihira, it is not possible to use a rigid sealing material because of the difficulty

of dispersing the fillers uniformly over the wafer. In the present invention, on the other hand, use of the rigid sealing material is possible because of the use of the wafer-level compressional molding process. The "rigid sealing material" means a sealing resin containing a large amount of fillers.

It may be the Examiner's position that the sealing material of Kihira would be "rigid" after cooling. However, Kihira does not teach the claimed step of supplying a rigid sealing material, since the sealing material 19 of Kihira would not be rigid when it is supplied in its encapsulating step.

Claims 65-67 and 69 were rejected under 35 U.S.C. §102(b) as being anticipated by Herndon. Favorable reconsideration of this rejection is requested in view of the amendments made herein.

More specifically, claim 65 has been amended to specify that the sealing resin forming step is conducted by providing a film between the electrode plate and a mold. By using a film, the electrode on the electrode plate is urged into the film at the time of the sealing process, and it becomes possible to ensure exposure of the electrode on the sealing resin layer. Herndon fails to teach or suggest use of a film in the sealing step.

Claim 86 was rejected under 35 U.S.C. §102(b) as being anticipated by Yamaji. This rejection is respectfully traversed.

The Examiner appears to have mischaracterized Yamaji as providing a semiconductor device main body having a resin layer which is formed on the surface of the semiconductor element which seals the protruding electrodes except for ends thereof. In Fig. 3A of Yamaji, it is clearly shown that the layer 4 is not formed on the semiconductor device main body 1. Thus, at least for this reason, the anticipation rejection should be withdrawn. It is noted that the Examiner also considers the layer 4 as corresponding to an adhesive used in the claimed bonding step of bonding the semiconductor

device main body and the interposer by an adhesive.

Claim 78 was rejected under 35 U.S.C. §103(a) as being unpatentable over Yamaji further in combination with Pennisi. This rejection is respectfully traversed.

Pennisi fails to provide the teachings which Yamaji lacks, as noted above.

Claim 90 was rejected under 35 U.S.C. §103(a) as being unpatentable over the combination of Ota and Kihira. Favorable reconsideration of this rejection is earnestly solicited.

Claim 90 has been amended to specify that the protruding electrodes and the mold, which thus contacts the sealing resin through the film. Thus, for the same reasons discussed above, the cited art fails to teach or suggest the features of amended claim 90.

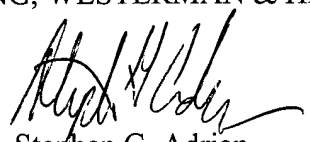
For at least the foregoing reasons, the claimed invention distinguishes over the cited art and defines patentable subject matter. Favorable reconsideration is earnestly solicited.

Should the Examiner deem that any further action by applicants would be desirable to place the application in condition for allowance, the Examiner is encouraged to telephone applicants' undersigned attorney.

In the event that this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,

ARMSTRONG, WESTERMAN & HATTORI, LLP



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Attachment: Version with markings to show changes made

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